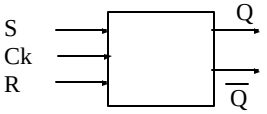
Lecture 22: Sequential Circuits

- Latches:
  - SR
  - D
  - JK
- Flip-Flops
- Memory

Sequential Circuits

- In sequential circuits, new state depends on not only the input, but also on the previous state.

S-R Latch (Clocked)



S = Set
R = Reset
Ck = Clock (enable)
Q = state of the latch

2 inputs (+ clock pulse)
2 outputs which are complements of each other.

The state of the latch is allowed to change with time (allowed to change when clock pulse goes to one)

Characteristic Table, SR Latch

- Characteristic table specifies next state when inputs and present state are known:

Excitation Table, SR Latch

- Excitation table: lists required input combinations for a given change of state.
  a) create column for each possible state change
  b) use characteristic table to figure out inputs.

SR - Summary

- When the clock pulse changes from 0 to 1, AND

- So, set latch in a certain state by passing inputs 01 or 10. Once in a state, keep it there by sending 00.
- Inputs (S&R) get passed to circuit only when the clock pulse = 1.

SR Latch Implementation

- Clock – either circuitry or driven by quartz crystal oscillator.

- Goal – produce a circuit that can remember.

S-R Timing Diagram

- A convenient way to visualize sequential circuits is with a timing diagram:

Problem with S-R

- What happens when S=R=1?
  - When S=R=1, Q = notQ = 0
- So what happens if it drops back to S=R=0?
- We need a circuit where S=R=1 is not possible!

Clocked D Latch

- Only one input (besides clock); the input goes into one AND gate and it's complement into the other AND gate.
- When clock=1, the current value of D is sampled and stored in the latch.
- When clock=0, the latch "remembers" (holds its last value)
- This is how most memories work (this is a one-bit memory)

Characteristic Table, D Latch

- Characteristic table specifies next state when inputs and present state are known:

D Latch as Memory

- To "remember" the last output (read memory) either:
  - disable the clock input or,
  - feed output back into the input so that clock pulses keep the state of the latch unchanged.
- To write memory, set or clear the D input to the value and the next clock pulse will load the current value of D into memory.

J-K Latch

- Like an S-R latch, except 1-1 is also a valid input.

- 1-1 is the toggle function. It outputs the complement of the state before the clock pulse.
- Versatile and useful. Used to implement counters.

Latches vs. Flip-Flops

- A Latch constantly computes its result (in the case of D, stores its input) while the CK input is 1. I.e., it acts as a combinational circuit while CK-1.
- A Flip-Flop is an edge triggered device: the value stored in the flip flop is only changed when CK changes from 0 to 1 (rising edge triggered) or 1 to 0 (falling edge triggered)
- If the input changes while CK=1, a latch and a flip-flop produce different outputs.

Pulse Generator

D Latches and Flip-Flops

- Figure 3-27, Tannenbaum
- Figure 3-38, Tannenbaum

Memory

- Figure 3-29 from Tannenbaum

Memory Chips

Random Access Memory

- RAM (Random Access Memory)
  - static –
  - dynamic (DRAM) –
- Why use DRAM?
- DRAM is slower though.
- Typical configuration:
  - DRAM main memory
  - Static RAM cache

Read Only Memory

- Hold programs and data that are never changed and that must remain stored even if the power is turned off.
- ROM –
- PROM –
- EPROM –
- EEPROM –
- Flash Memory –

Memory Type Comparison

- Figure 3-32, Tannenbaum